AMENDMENTS TO THE CLAIMS

Claims 1-6 (Cancelled)

7. (Original) A method of forming a semiconductor device, the method comprising the steps of:

forming a layer of insulation material over a semiconductor substrate, the layer of insulation material having a first opening that defines a first side wall and an opposing second side wall;

forming a first layer of conductive material on the layer of insulation material to fill up the first opening;

anisotropically etching the first layer of conductive material to form a first conductive spacer that adjoins the first side wall and the second side wall, and a second opening;

forming a first layer of isolation material on the layer of insulation material and the first conductive spacer to fill up the second opening; and

forming a conductive region on the first conductive spacer and the first layer of isolation material, the conductive region making an electrical connection with the first conductive spacer.

8. (Original) The method of claim 7 and further comprising the steps of:

anisotropically etching the first layer of isolation material to form a first isolation spacer that adjoins the first conductive spacer, and a third opening;

forming a second layer of conductive material on the layer of insulation material to fill up the third opening;

anisotropically etching the second layer of conductive material to form a second conductive spacer that adjoins the first isolation spacer, and a fourth opening;

forming a second layer of isolation material on the layer of insulation material and the first conductive spacer to fill up the fourth opening,

the conductive region making an electrical connection with the first and second conductive spacers.

9. (Original) The method of claim 7 and further comprising the step of planarizing the layer of insulation material, the first conductive spacer, and the first layer of isolation material until the layer of insulation material, the first conductive spacer, and the first layer of isolation material have a substantially planar top surface.

10. (Original) The method of claim 8 and further comprising the step of planarizing the layer of insulation material, the first conductive spacer, and the first layer of isolation material until the layer of insulation material, the first conductive spacer, and the first layer of isolation material have a substantially planar top surface.

11. (Original) The method of claim 7 wherein the step of forming a conductive region includes the steps of:

forming a second layer of conductive material on the layer of insulation material, the first conductive spacer, and the first layer of isolation material;

forming a mask on the second layer of conductive material that exposes regions of the second layer of conductive material; and

etching the exposed regions of the second layer of conductive material.

12. (Original) The method of claim 8 wherein the step of forming a conductive region includes the steps of:

forming a third layer of conductive material on the layer of insulation material, the first conductive spacer, the first layer of isolation material, and the second conductive spacer;

forming a mask on the third layer of conductive material that exposes regions of the third layer of conductive material; and

etching the exposed regions of the third layer of conductive material.

13. (Original) The method of claim 7 wherein the first opening is formed to have a number of loops.

Claims 14-15 (Cancelled)

16. (New) A method of forming a semiconductor device on an insulation region, the insulation region having a top surface, the method comprising the steps of:

forming a trench in the insulation region, the trench having a side wall surface and a bottom surface;

forming a layer of conductive material on the insulation region to fill up the trench; and

etching the layer of conductive material to remove the layer of conductive material from the top surface of the insulation region, and form an opening and a conductive spacer that contacts the side wall surface.

17. (New) The method of claim 16 and further comprising the step of forming a layer of isolation material on the insulation region and the conductive spacer to fill up the opening.

18. (New) The method of claim 17 and further comprising the steps of:

etching the layer of isolation material to remove the layer of isolation material from the top surface of the insulation region and expose the conductive spacer; and

forming a conductive region on the conductive spacer and the layer of isolation material, the conductive region making an electrical connection with the conductive spacer.

19. (New) The method of claim 17 and further comprising the steps of:

etching the layer of isolation material to form a hole and an isolation spacer that contacts a side wall of the conductive spacer; and

forming a layer of conducting material on the insulation region, the conductive spacer, and the isolation spacer to fill up the hole.

20. (New) The method of claim 19 and further comprising the steps of:

etching the layer of conducting material to remove the layer of conducting material from the top surface of the insulation region, wherein a top surface of the conductive spacer is exposed during an etch; and

forming a conductive region on the conductive spacer, the isolation spacer, and the conducting material in the hole, the conductive region making an electrical connection with the conductive spacer and the conducting material.

21. (New) The method of claim 19 and further comprising the steps of:

etching the layer of conducting material to remove the layer of conducting material from the top surface of the insulation region, and form an aperture and a conducting spacer that contacts a side wall of the isolation spacer; and

forming a layer of insulation material on the insulation region, the conductive spacer, the isolation spacer, and the conducting spacer to fill up the aperture.

22. (New) The method of claim 21 and further comprising the steps of:

etching the layer of insulation material to remove the layer of insulation material from the top surface of the insulation region, wherein a top surface of the conductive spacer and a top surface of the conducting spacer during an etch; and

forming a conductive region on the conductive spacer, the isolation spacer, the conducting spacer, and the layer of insulation material in the aperture, the conductive region making an electrical connection with the conductive spacer and the conducting spacer.

23. (New) The method of claim 17 and further comprising the steps of:

planarizing the insulation region, the conductive spacer, and the layer of isolation material until the layer of insulation material, the conductive spacer, and the layer of isolation material have a substantially planar top surface; and

forming a conductive region on the conductive spacer and the layer of isolation material, the conductive region making an electrical connection with the conductive spacer.

24. (New) The method of claim 19 and further comprising the steps of:

planarizing the insulation region, the conductive spacer, the isolation spacer, and the layer of conducting material until the insulation region, the conductive spacer, the isolation spacer, and the layer of conducting material have a substantially planar top surface; and

forming a conductive region on the conductive spacer, the isolation spacer, and the layer of conducting material, the conductive region making an electrical connection with the conductive spacer and the layer of conducting material.

25. (New) The method of claim 18 wherein the trench is formed to have a number of loops.

26. (New) The method of claim 18 wherein the opening exposes the bottom surface of the trench.

27. (New) The method of claim 19 wherein the hole exposes the bottom surface of the trench.